MULTI-SPEED DELAY-LOCKED LOOP

ABSTRACT

A delay locked loop includes a primary delay line having a plurality of series-connected delay elements, wherein each of the delay elements operates in response to a supply voltage provided on a voltage supply line. When the delay locked loop is configured to operate in response to an input clock signal having a relatively high frequency, the voltage supply line is coupled to receive a first supply voltage. When the delay locked loop is configured to operate in response to an input clock signal having a relatively low frequency, the voltage supply line is coupled to receive a second supply voltage, which is significantly lower than the first supply voltage. When operating in response to the first supply voltage, the delay elements exhibit relatively short delays. Conversely, when operating in response to the second supply voltage, the delay elements exhibit relatively long delays.